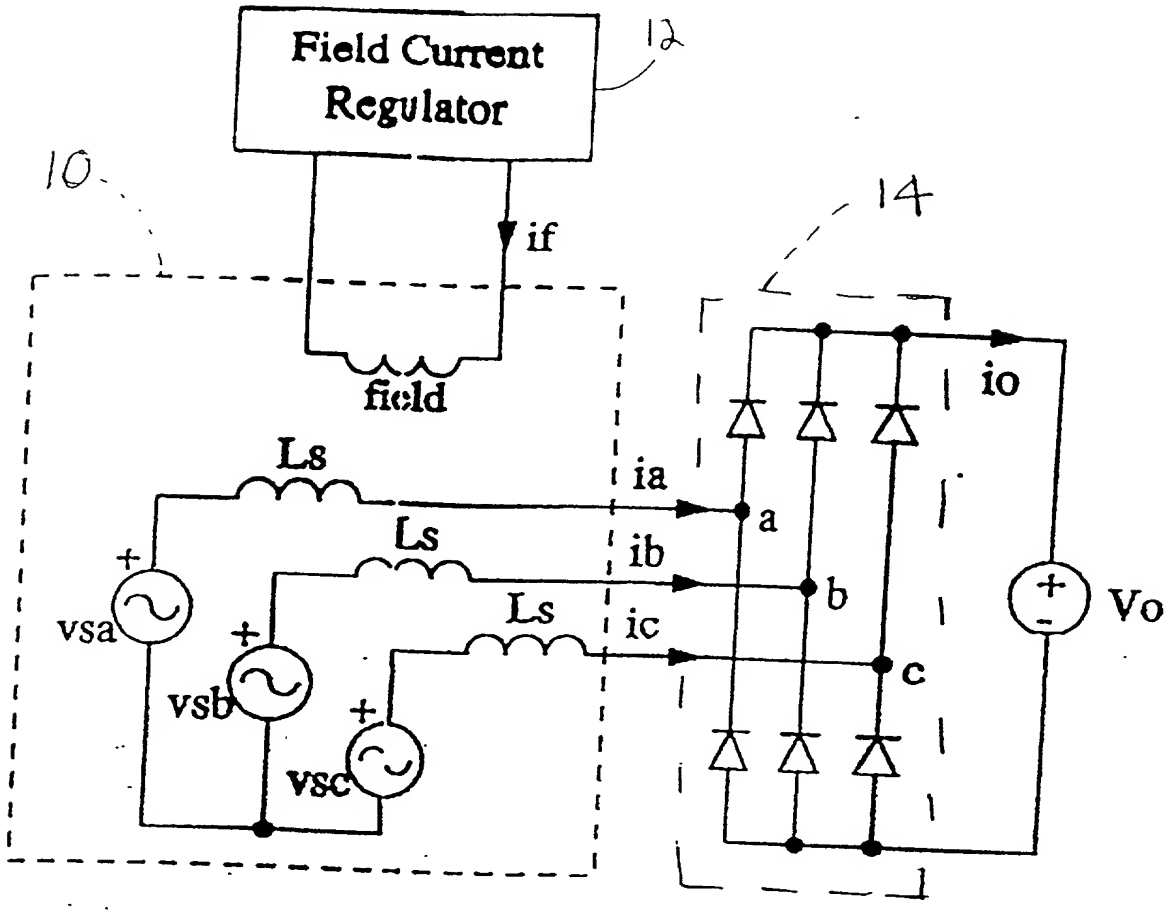
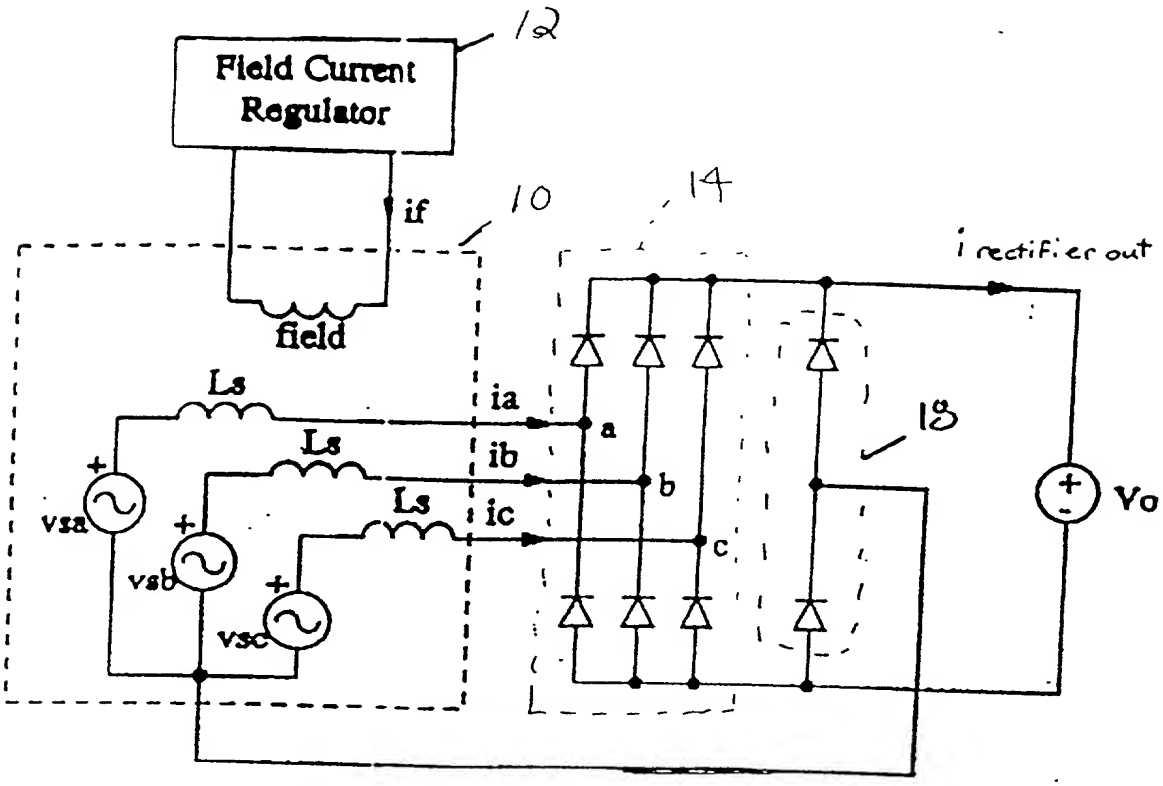



PRIOR ART

FIG. 1A




PRIOR ART

FIG. 1B

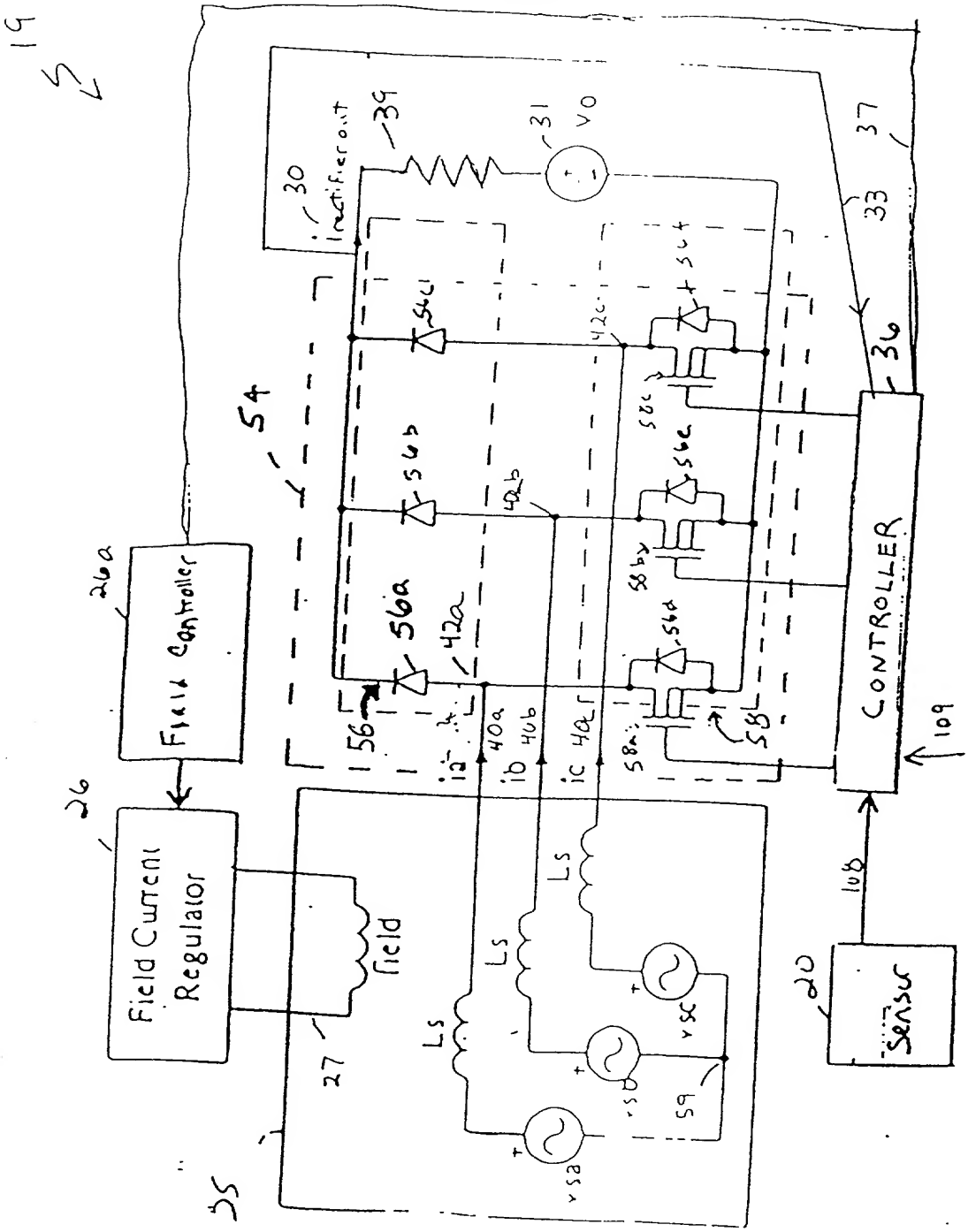

19
30
Rectifier unit
39
31
VO
37
33
36
54
54a
54b
54c
54d
42a
42b
42c
56a
56b
56c
56d
58a
58b
58c
58d
58
56
ia
ib
ic
40a
40b
40c
CONTROLLER
109
26a
Field Controller
26
Field Current Regulator
27
Field
Ls
Ls
Ls
35
VSa
VSb
VSc
59
108
20
Sensor

FIG. 2

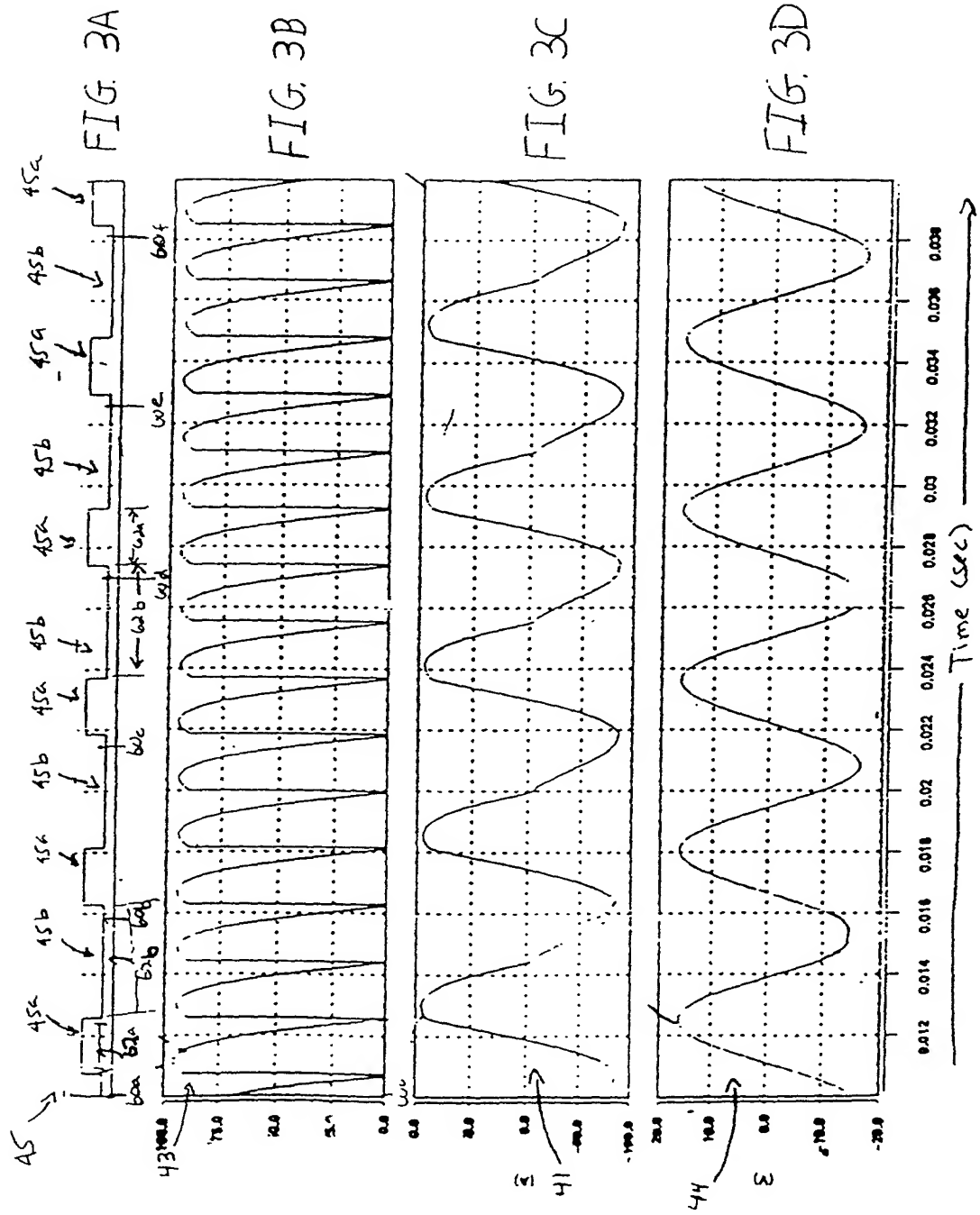


FIG. 3A
FIG. 3B
FIG. 3C
FIG. 3D
Time (sec)

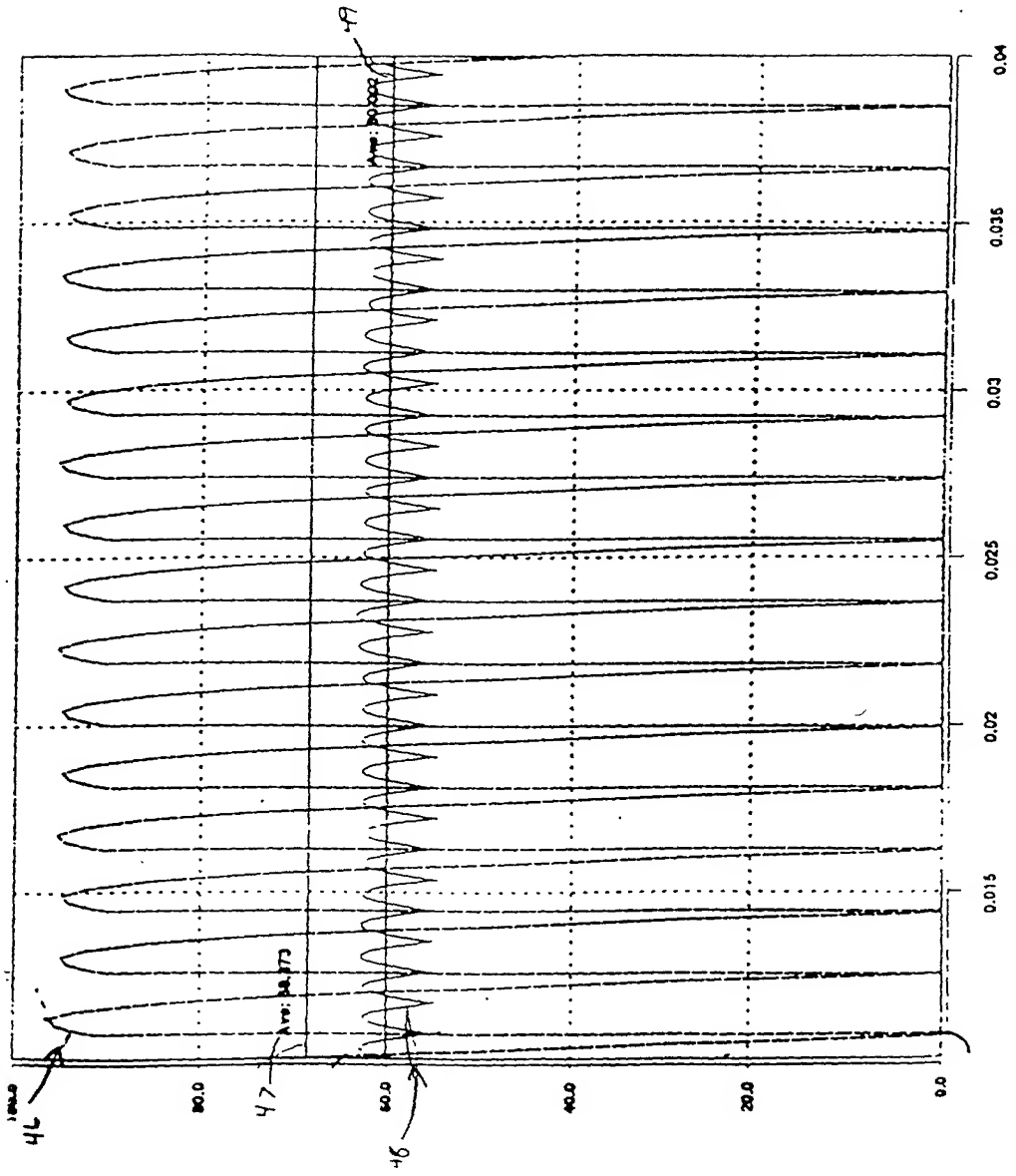



FIG. 4

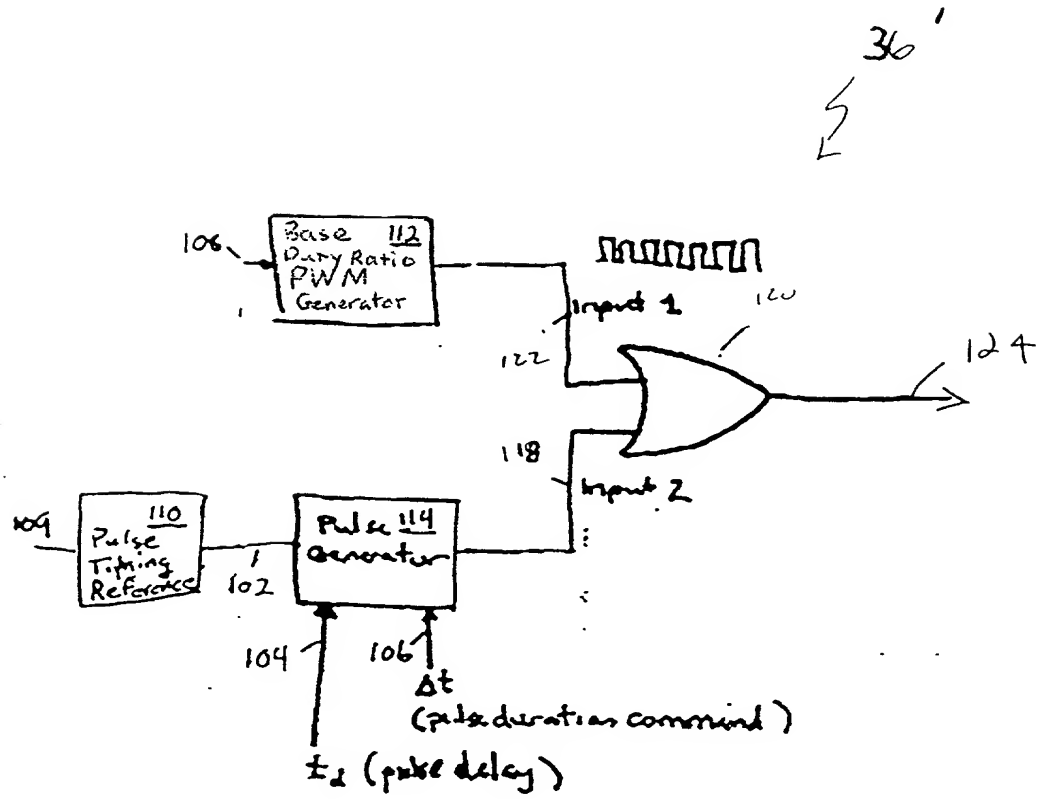

36'
106
Base 112
Duty Ratio
PWM
Generator
Input 1
120
122
124
118
Input 2
109
110
Pulse
Timing
Reference
102
Pulse 114
Generator
104
106
Δt
(pulse duration command)
$t_d$ (pulse delay)

FIG. 5

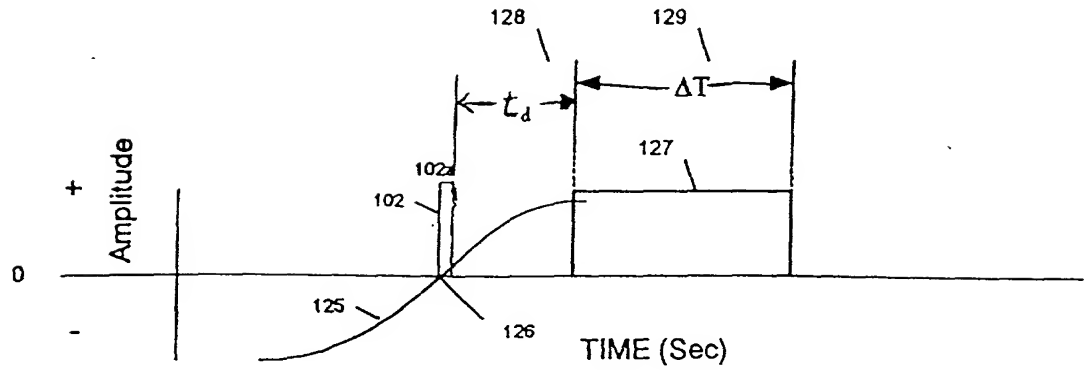

128
129
$t_d$
ΔT
127
102a
102
+
Amplitude
0
-
125
126
TIME (Sec)

FIG. 6A

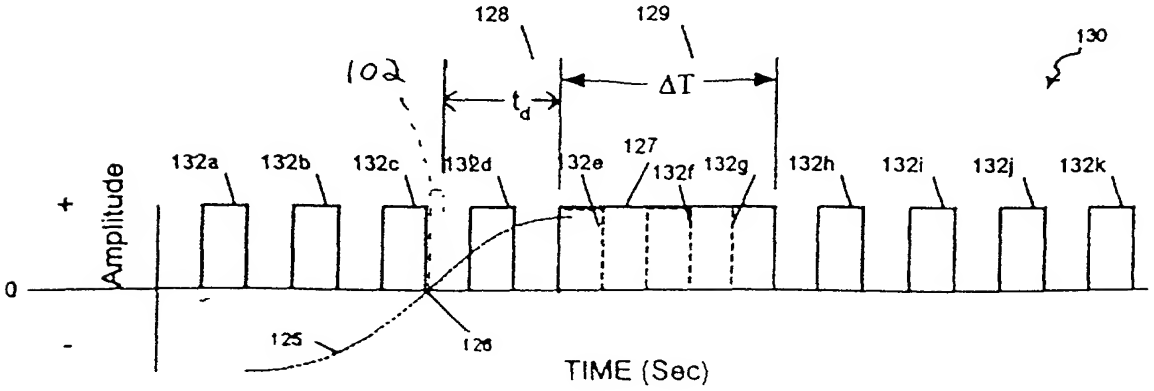

128
129
130
102
$t_d$
ΔT
127
132a
132b
132c
132d
132e
132f
132g
132h
132i
132j
132k
+
Amplitude
0
-
125
126
TIME (Sec)

FIG. 6B

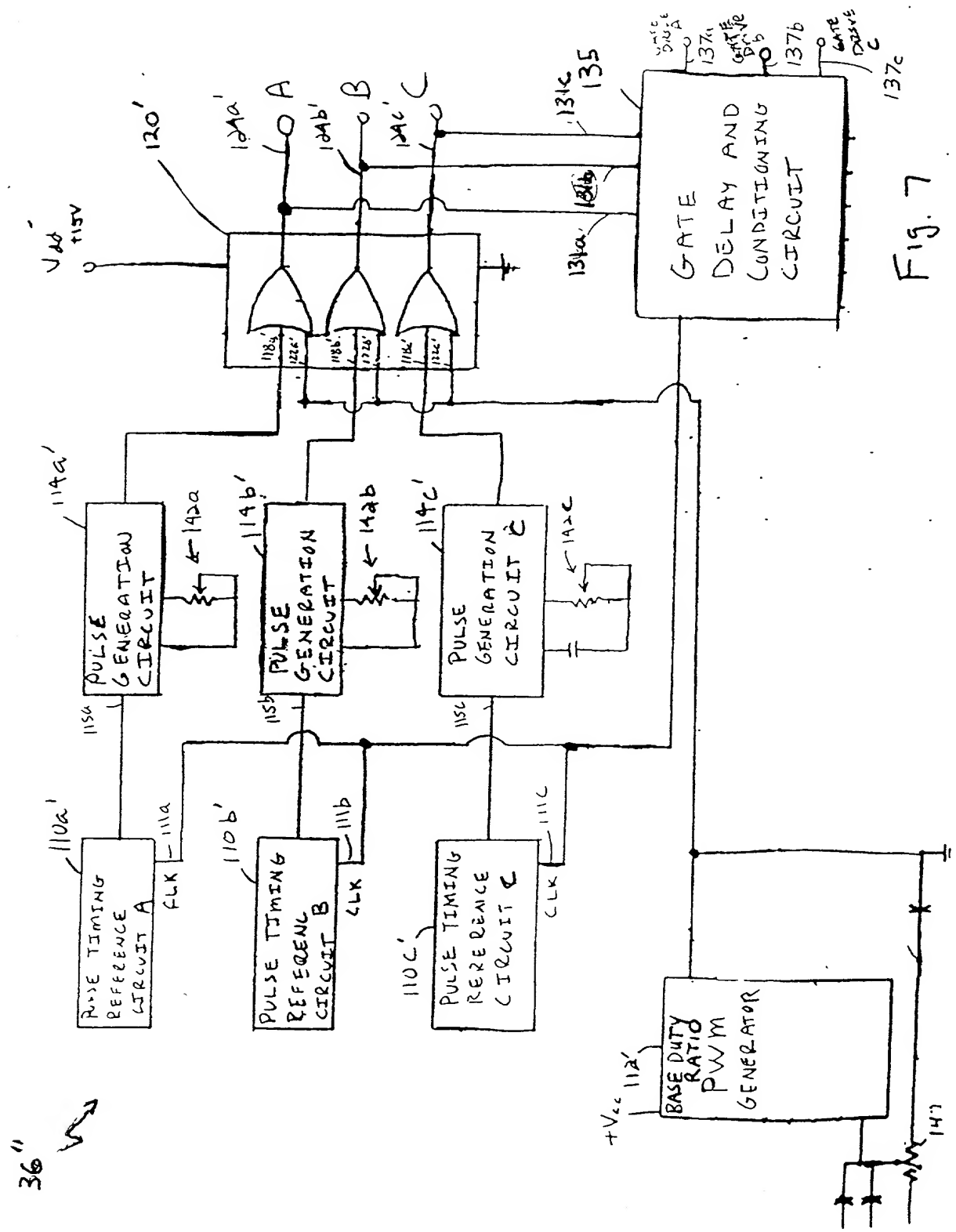

GATE DELAY AND CONDITIONING CIRCUIT
PULSE GENERATION CIRCUIT A
PULSE GENERATION CIRCUIT B
PULSE GENERATION CIRCUIT C
PULSE TIMING REFERENCE CIRCUIT A
PULSE TIMING REFERENCE CIRCUIT B
PULSE TIMING REFERENCE CIRCUIT C
BASE DUTY RATIO PWM GENERATOR
CLK
+15V
+Vcc
120'
135
36'

Fig. 7

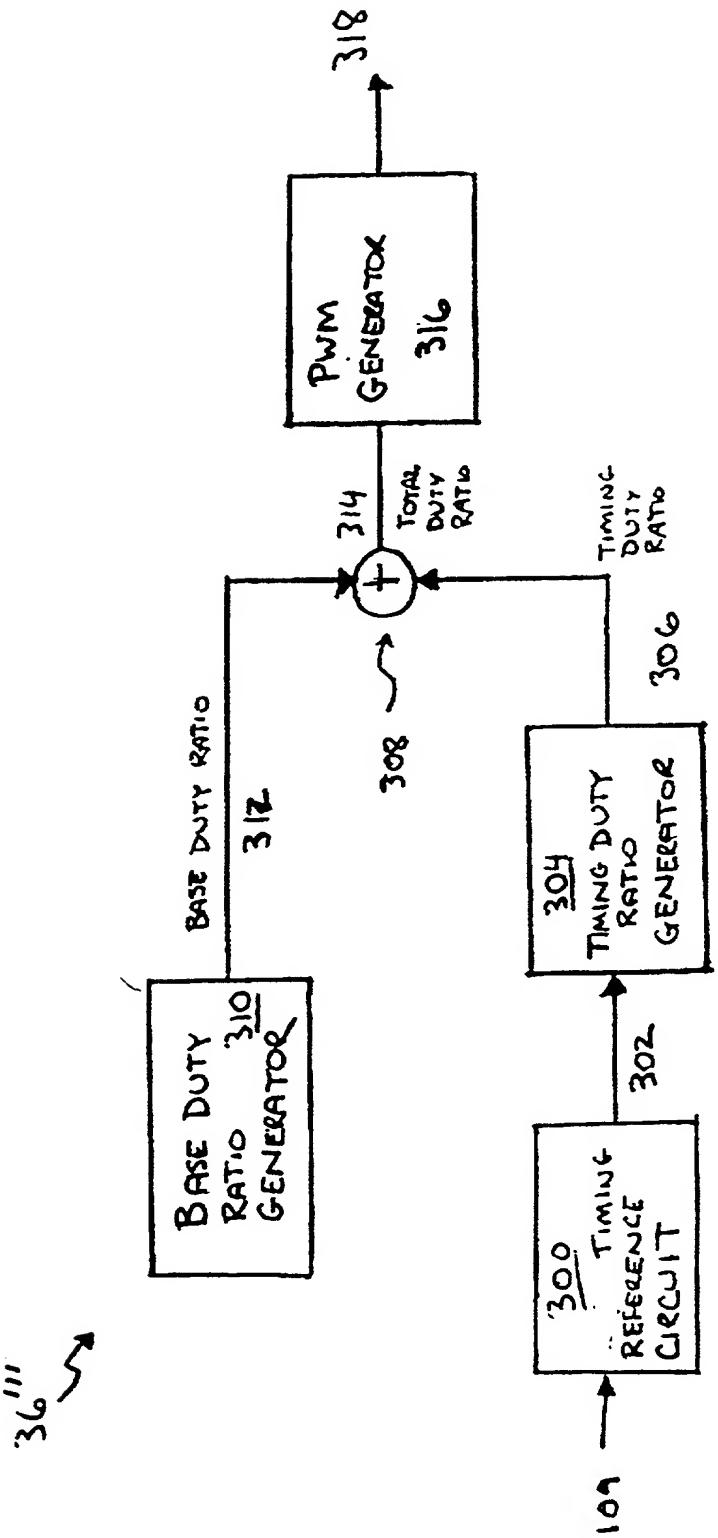

318
PWM GENERATOR 316
314
TOTAL DUTY RATIO
TIMING DUTY RATIO
306
308
BASE DUTY RATIO
312
BASE DUTY RATIO GENERATOR 310
304 TIMING DUTY RATIO GENERATOR
302
300 TIMING REFERENCE CIRCUIT
109
36'''

FIG. 8

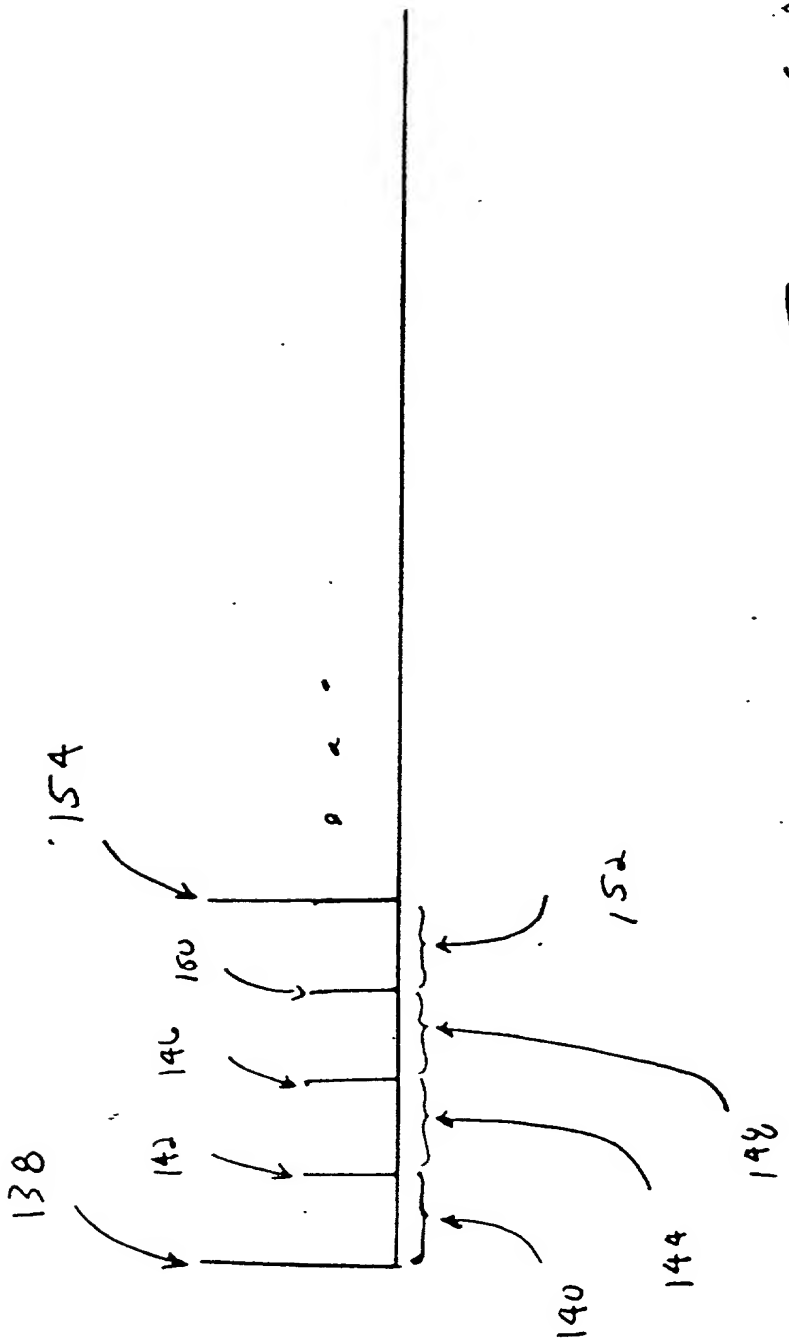



Fig. 8A

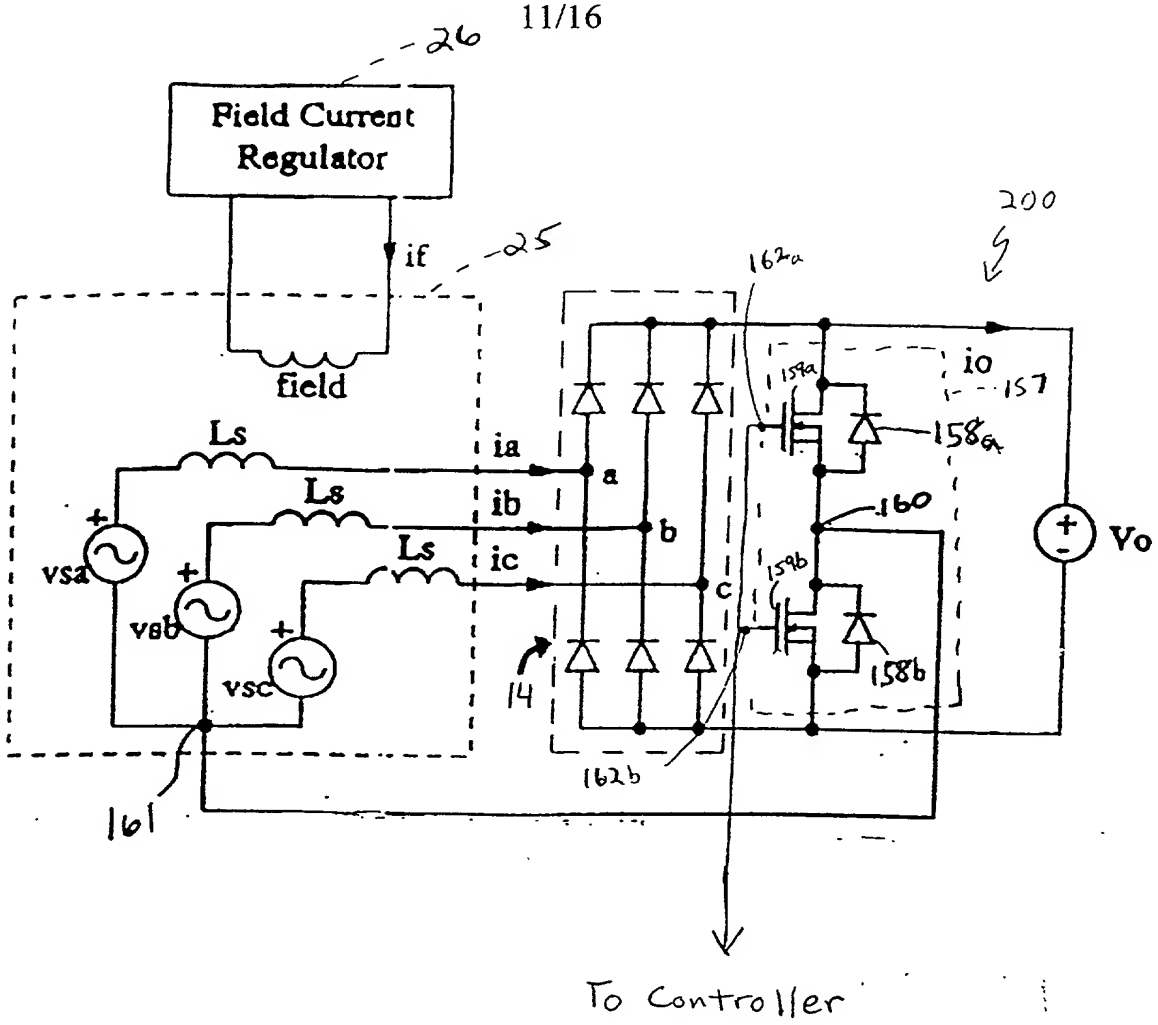

26
Field Current Regulator
if
25
field
200
162a
io
157
158a
158a
160
Ls
ia
a
Ls
ib
b
Ls
ic
c
vsa
vsb
vsc
14
159b
158b
Vo
161
162b
To Controller

Fig. 9

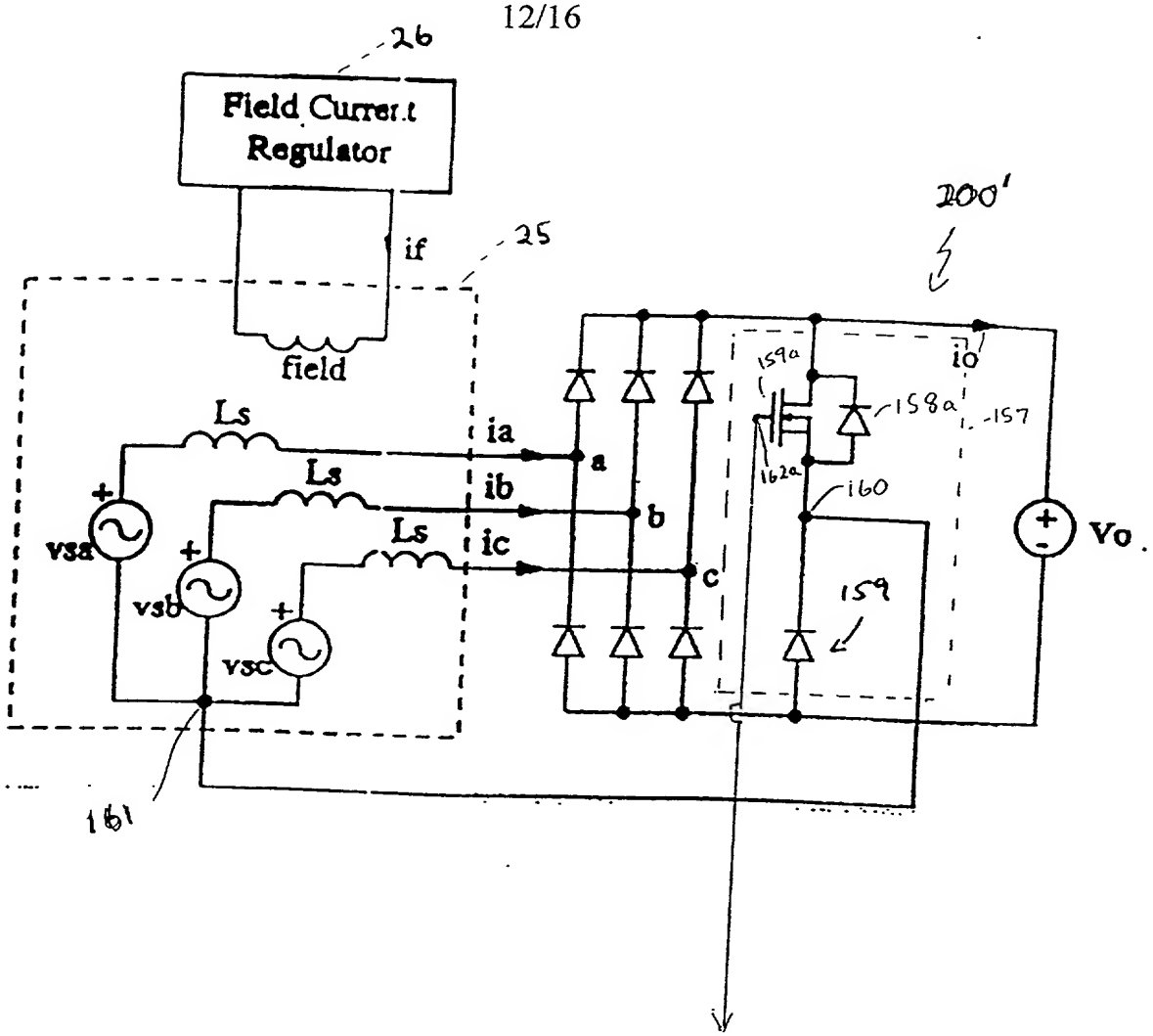

26
Field Current Regulator
if
25
field
200'
Ls
Ls
Ls
ia
ib
ic
a
b
c
vsa
vsb
vsc
159a
158a
157
162a
160
159
io
Vo
161
To Controller

Fig. 10

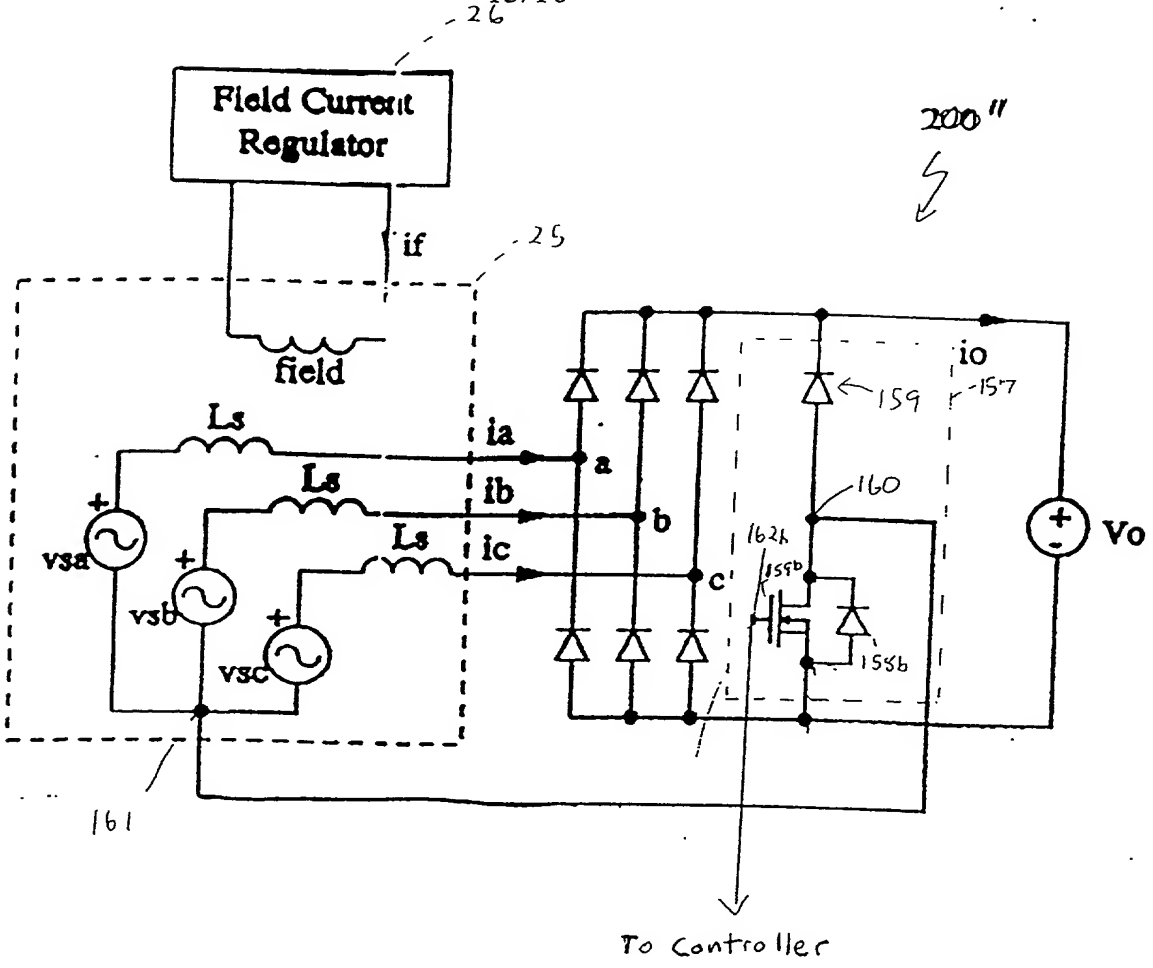
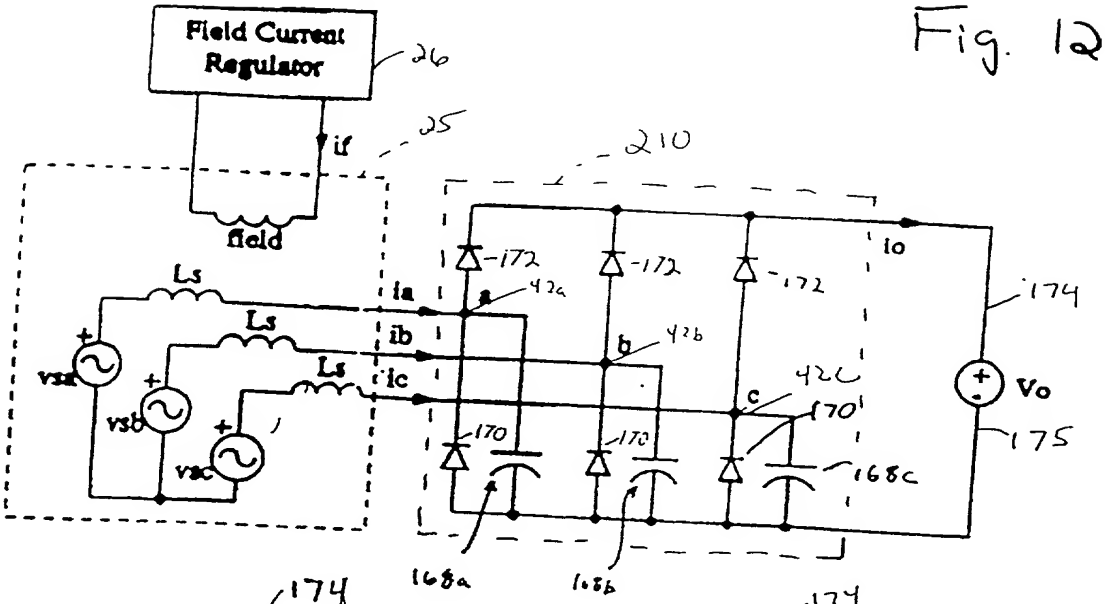

26
Field Current Regulator
200"
if
25
field
Ls
Ls
Ls
ia
ib
ic
a
b
c
vsa
vsb
vsc
161
io
159
157
160
162a
155b
158b
Vo
To Controller

Fig. 11

Fig. 12



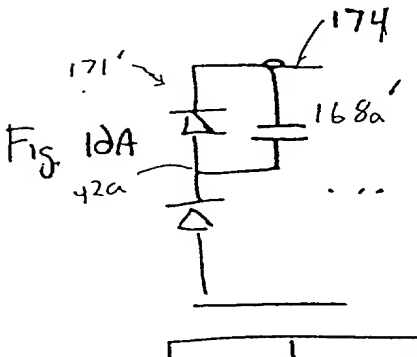




Fig 12A

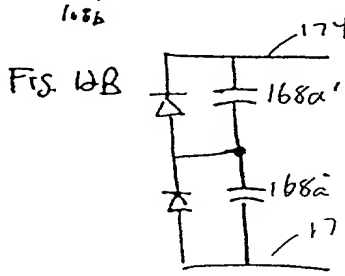



Fig 12B

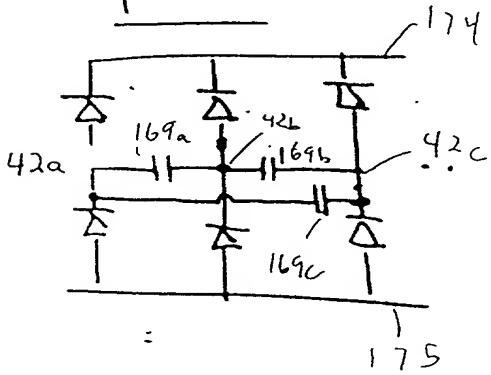



Fig 12C

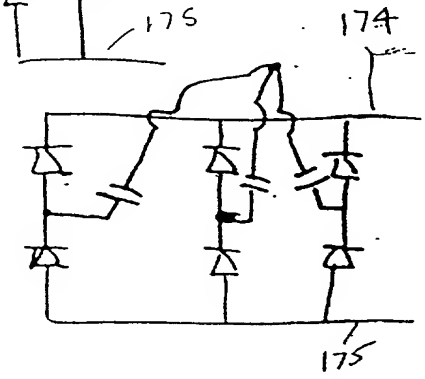



FIG 12D

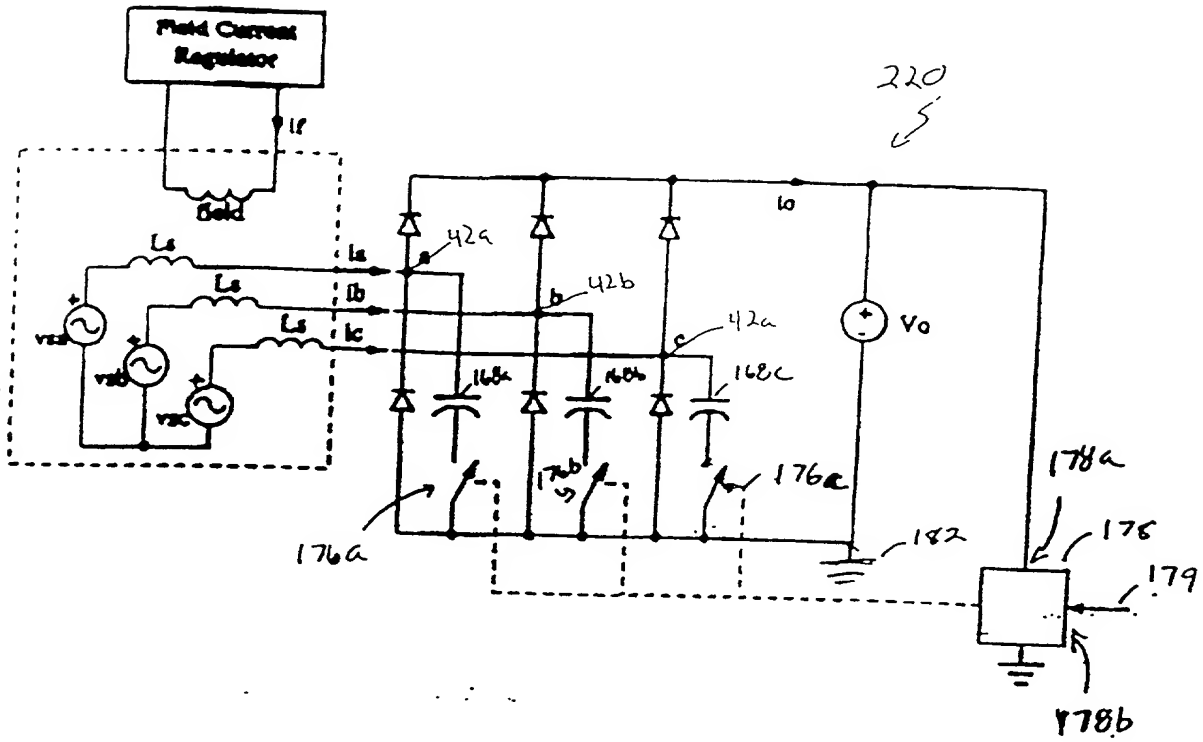
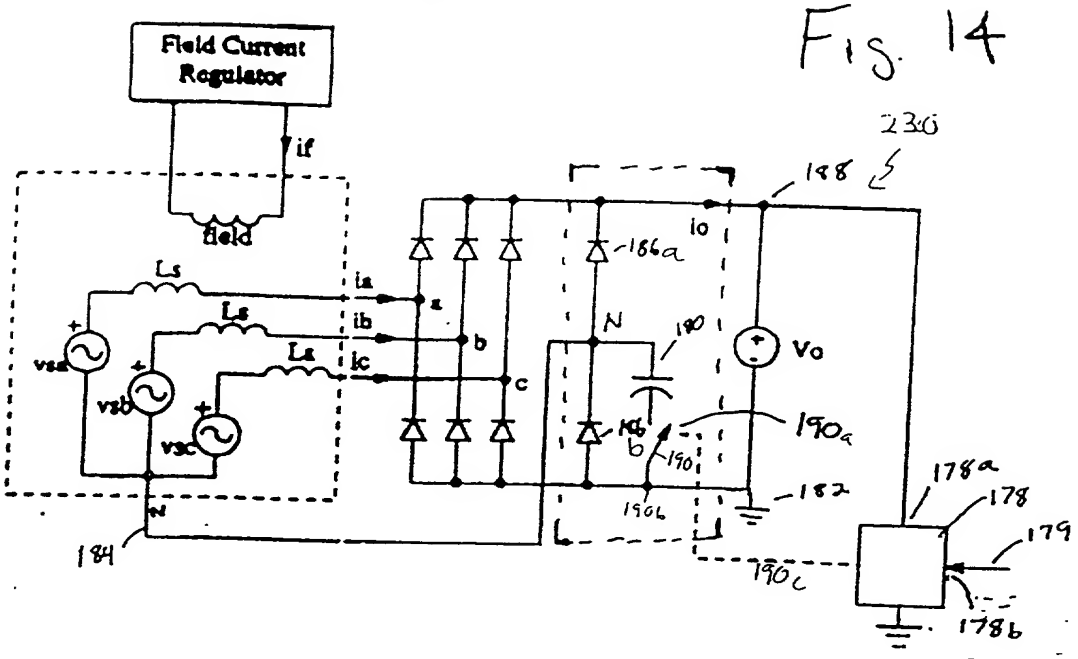



Fig. 13

Patent No. 5,929,605

Fig. 14



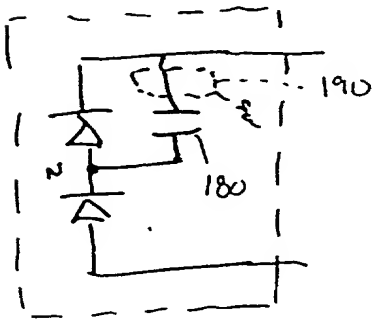




Fig. 14A

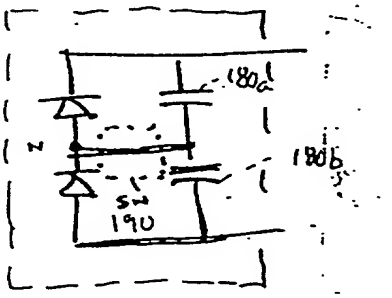



Fig. 14B

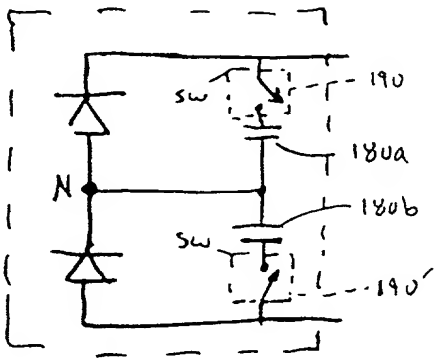



Fig. 14C